CLAIMS

1. A cache memory system for storing blocks of graphics data in a graphics processing system, the cache memory system comprising:

a first memory to store an address and an associated ID number for each block of graphics data stored in the cache memory, the address corresponding to a storage location in the cache memory and the associated ID number assigned to distinguish between blocks of graphics data having the same address;

a comparator coupled to the first memory to generate a signal in response to receiving a requested address and ID number for graphics data matching one of the addresses and associated ID numbers stored in the first memory; and

a second memory coupled to the comparator to provide the block of graphics data corresponding to the matching address and associated ID number in response to receiving the signal.

2. The cache memory of claim 1 wherein the first memory comprises a tag cache to store the address of each block of graphics data and an ID cache to store the associated ID number.

3. The cache memory of claim 1 wherein the second memory comprises a data cache.

4. The cache memory of claim 1 wherein the comparator is included in a cache controller coupled to the first and second memories.

5. The cache memory of claim 1 wherein the associated ID number is assigned to the blocks of graphics data when written to the memory and corresponds to a

frame number of a graphics frame in which the blocks of graphics data is first used for rendering.

6. The cache memory of claim 1, further comprising an invalidation circuit coupled to the first memory to reset the addresses and associated ID numbers in the first memory to a predetermined value.

7. A cache memory for storing graphics data in a graphics processing system, the cache memory comprising:

a first memory means for storing addresses corresponding to memory addresses at which the graphics data is stored;

a second memory means for storing an ID number associated with the graphics data for each address stored in the first memory means;

a comparator means coupled to the first and second memories for generating a hit signal in response to receiving an address and ID number for requested graphics data matching an entry stored in the first and second memory means, respectively; and

a data cache means coupled to the comparator for providing the graphics data corresponding to the matching address and ID number in response to receiving the hit signal.

8. The cache memory of claim 7 wherein the comparator means is included in a cache controller coupled to the first and second memory means.

9. The cache memory of claim 7, further comprising an invalidation circuit coupled to the first memory to reset the addresses and associated ID numbers in the first memory to a predetermined value.

10. A computer system, comprising:

a central processing unit;

a system memory coupled to the CPU;

a bus coupled to the CPU; and

a graphics processing system coupled to the bus having a graphics processor assigning ID numbers to blocks of graphics data stored in the system memory and a graphics processing stage receiving a requested address and ID number for graphics data from the graphics processor, the graphics processing stage including a cache memory for storing blocks of graphics data written to the system memory, the cache memory comprising:

a first memory to store an address and an associated ID number for each block of graphics data stored in the cache memory, the address corresponding to a storage location in the system memory and the associated ID number assigned by the graphics processor to distinguish between blocks of graphics data having the same address;

a comparator coupled to the first memory to generate a signal in response to receiving a requested address and ID number from the graphics processor for graphics data matching one of the addresses and associated ID numbers stored in the first memory; and

a second memory coupled to the comparator to provide the block of graphics data corresponding to the matching address and associated ID number in response to receiving the signal.

11. The computer system of claim 10 wherein the first memory comprises a tag cache to store the address of each block of graphics data and an ID cache to store the associated ID number.

12. The computer system of claim 11 wherein the second memory comprises a data cache.

13. The computer system of claim 11 wherein the comparator is included in a cache controller coupled to the first and second memories.

14. The computer system of claim 11 wherein the associated ID number is assigned to the blocks of graphics data when written to the memory and corresponds to a frame number of a graphics frame in which the blocks of graphics data is first used for rendering.

15. The computer system of claim 11, further comprising an invalidation circuit coupled to the first memory to reset the addresses and associated ID numbers in the first memory to a predetermined value.

16. A computer system, comprising:

a central processing unit;

a system memory coupled to the CPU;

a bus coupled to the CPU; and

a graphics processing system coupled to the bus having a graphics processor assigning ID numbers to blocks of graphics data stored in the system memory and a graphics processing stage receiving a requested address and ID number for graphics data from the graphics processor, the graphics processing stage including a cache memory for storing blocks of graphics data written to the system memory, the cache memory retrieving the cached graphics data by:

comparing the requested address and ID number to stored entries in a first memory having an address tag and associated ID number; and

providing from a second memory graphics data corresponding to one of the stored entries having an address tag and an associated ID number matching the requested address and ID number.

17. The computer system of claim 16 wherein the cache memory retrieves the cached graphics data by further:

retrieving from a third memory a retrieved graphics data corresponding to the requested address and ID number in response to a stored entry having an address tag matching the requested address but an associated ID number not matching the requested ID number;

replacing in the first memory the associated ID number for the stored entry and the corresponding graphics data in the second memory with the retrieved graphics data; and

providing from the second memory the retrieved graphics data.

18. The computer system of claim 16 wherein the ID number assigned to blocks of graphics data stored in the system memory comprises a value corresponding to a frame number for a graphics frame being rendered when the blocks of graphics data are written to the system memory.

19. A method of caching blocks of graphics data stored in a memory, comprising:

assigning an ID number to blocks of graphics data stored in the memory, the ID number distinguishing between blocks of graphics data presently and formerly stored in the memory;

storing a tag and an ID number for each cached block of graphics data;

comparing a requested tag and ID number to the stored tags and ID numbers; and

providing the cached block of graphics data corresponding to the tag and ID number matching the requested tag and ID number.

20. The method of claim 19 wherein assigning the ID number to blocks of graphics data stored in the memory comprises assigning a value to the blocks of graphics data when written to the memory corresponding to a frame number for which the block of graphics data is first referenced.

21. The method of claim 19 wherein assigning the ID number to the blocks of graphics data stored in the memory comprises assigning a unique value to blocks of graphics data

22. The method of claim 19, further comprising retrieving the block of graphics data from the memory corresponding to the requested tag and ID number when none of the stored tags and ID numbers match the requested tag and ID number.

23. A method of retrieving graphics data from a cache, comprising:

comparing a requested address and ID number to stored entries in a first memory having an address tag and associated ID number; and

providing from a second memory graphics data corresponding to one of the stored entries having an address tag and an associated ID number corresponding to the requested address and ID number.

24. The method of claim 23, further comprising:

retrieving from a third memory a retrieved graphics data corresponding to the requested address and ID number in response to a stored entry having an address tag matching the requested address but an associated ID number not matching the requested ID number;

replacing in the first memory the associated ID number for the stored entry and the corresponding graphics data in the second memory with the retrieved graphics data; and

providing from the second memory the retrieved graphics data.